# Next EU Vector Accelerators for World-Wide HPC Customers

NEC Users Group, Hamburg. June 12th 2024.

# Acronyms:

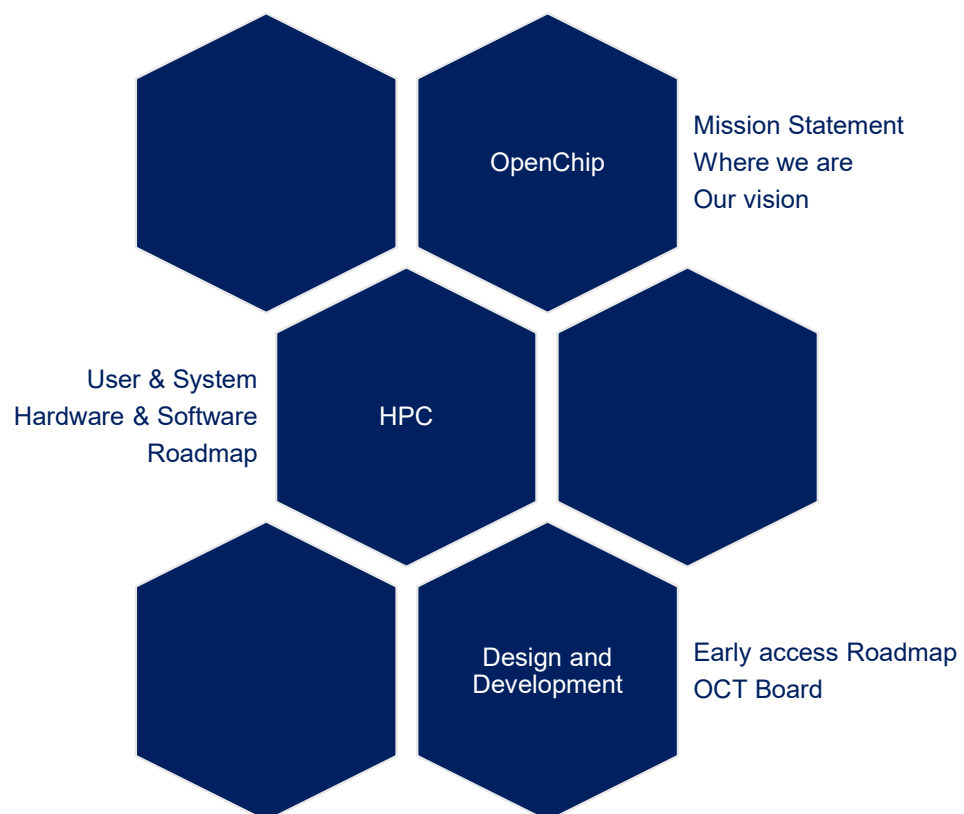IP:         *Intellectual Property*
SKU:        *Stock Keeping Unit (reference of a design of a Chip)*
SOC:        *System on Chip*
JV:         *Joint Venture*
SW:         *Software*
HPC:        *High Performance Computing*
OC:         *Openchip*
NewCo:      *New Company*
UCIe:       *Universal Chiplet Interconnect Express, open standard of interconnection of multiple Chiplets in a SOC.*
Chiplet:    *A tiny unit of an integrated circuit that contain a defined functionality.*
IoT:        *Internet of Things*
AI:         *Artificial Intelligence*
LLM:        *Large Language Models (of AI, as an example ChatGPT)*
BU:         *Business Unit*
RFx:        *Request for X, where X stands for (Information, Proposal, Quotation, Tender)*
ODM:        *Original Design Manufacturer*
OEM:        *Original Equipment Manufacturer*
IDM:        *Integrated Design Manufacturer*
ISV:        *Independent Software Vendor*
TEM:        *Telecommunications Equipment Manufacturer*
MOU:        *Memorandum of Understanding*
KPI:        *Key Performance Indicator*
R&D:        *Research and Development*
SI:         *System Integrator*
EDA:        *Electronic Design Automation (tool)*
CSP:        *Cloud Service Provider*

Other terms used:

Tape-out:   *Milestone that indicates the order to the fab to manufacture a Chip / SOC design.*
Edge:       *Segment of technology solutions located between the Connected Devices and the Cloud.*
Wafer:      *Disk of silicon where the chips are imprinted.*
Mask:       *Opaque plate with transparent areas that allow ultraviolet light to shine and project a Chip design into a wafer (similar to a diapositive in photography).*

# Agenda



OpenChip
- Mission Statement
- Where we are
- Our vision

HPC
- User & System
- Hardware & Software
- Roadmap

Design and Development
- Early access Roadmap
- OCT Board

# Agenda



OpenChip — Mission Statement / Where we are / Our vision

User & System / Hardware & Software / Roadmap — HPC

Design and Development — Early access Roadmap / OCT Board
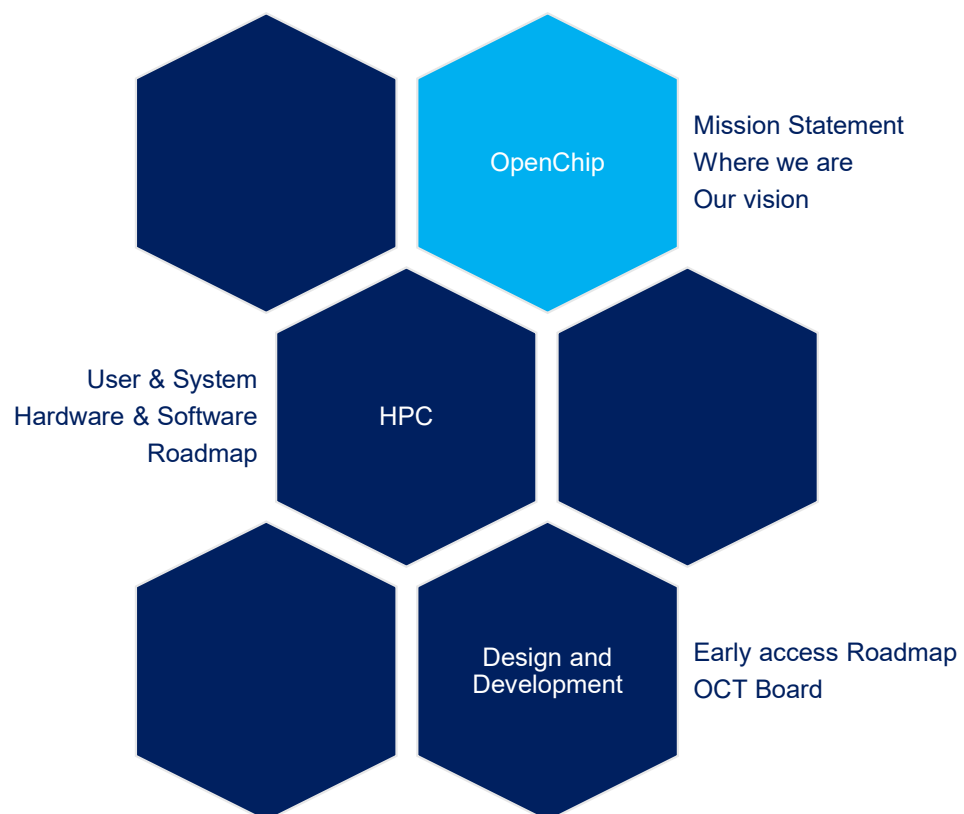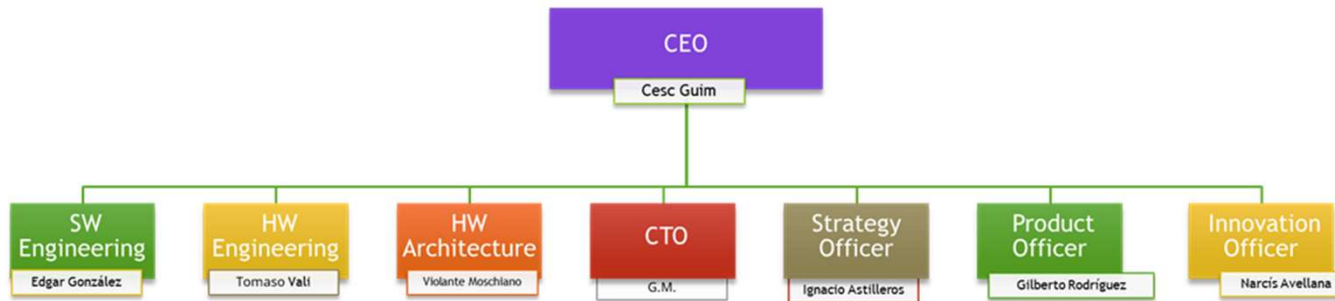
## 1. Who is Openchip?

OpenChip is a European silicon engineering company that aim to designs "system on chip" (SOC) for accelerated computing.

## 2. Where we are

We are located in Jordi Girona St. 29, Barcelona, Spain.



## 3. Our team

Our team includes +60 employees, we plan to be +120 by the end 2024 and up to 200 by 2025.

The executive team is highly experienced, counting with +1.000 patents, +200 years of experience in Intel, Micron, NEC, Infineon, Imagination, Nvidia, Google...



## 4. What do we want to do?

We aim to democratize the usage of chips by the adoption of open standards like RISC-V, UCIe to connect Chiplets, etc., combined with unique accelerators of Artificial Intelligence and Vector Processing; plus, a software stack based on open standards.

## 5. Which industries will benefit?

High performance computing, vector processing and artificial intelligence are being leveraged for intensive research activities in multiple domains of knowledge and science, like meteorological forecasting, protein design, astrophysics, oil & gas...

## 6. About Openchip & European Union

OpenChip is funded by the European Commission as a Project of Key Interest to support Research, Innovation and Development of the EU semiconductor industry, having board members from Spanish Government, BSC and GTD. Company supported with +€100M.

## 7. Our stakeholders

Our shareholders are Barcelona Supercomputing Center (BSC) and the leading engineering company GTD. We are headquartered in Barcelona, and our team is present across EU countries like Spain, Italy, Poland and Germany. Our technologies are designed to satisfy the demand of High-Performance Computing (HPC) , Artificial Intelligence (AI) and Vector Processing (VEC) and we count with a growing pipeline of customers.

**Shareholders, Board, etc**

GTD SYSTEM & SOFTWARE ENGINEERING

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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Enabling the Digital World

56%

44%

138M€
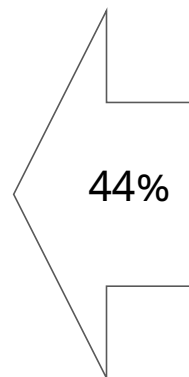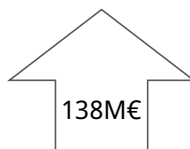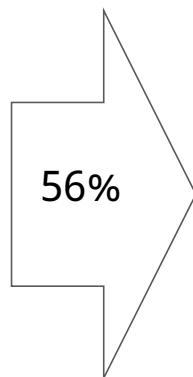
**Clients in 15 Countries - More than 1.500 high-tech projects**

GTD works across some of the most demanding industries, providing software, systems, and services for safety, mission, and business-critical applications. We provide our clients with secure, reliable technology around the world. Out in space, our software orbits the Earth 24/7, 365 days a year. Closer to home, our software keeps aircraft flying high, makes vehicles safer, powers smart meter networks, and does much more. For over **34 years**, we've been transforming the way the world uses technology.

PLAN DE RECUPERACIÓN, TRANSFORMACIÓN Y RESILIENCIA

European Commission

Gobierno de España, Ministerio de Ciencia, Innovación y Universidades
Generalitat de Catalunya Departament de Recerca i Universitats
UPC UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

EuroHPC Joint Undertaking

UNIÓN EUROPEA
Fondo Europeo de Desarrollo Regional
Una manera de hacer Europa

# Openchip Strategy to Contribute to EU Digital Sovereignty
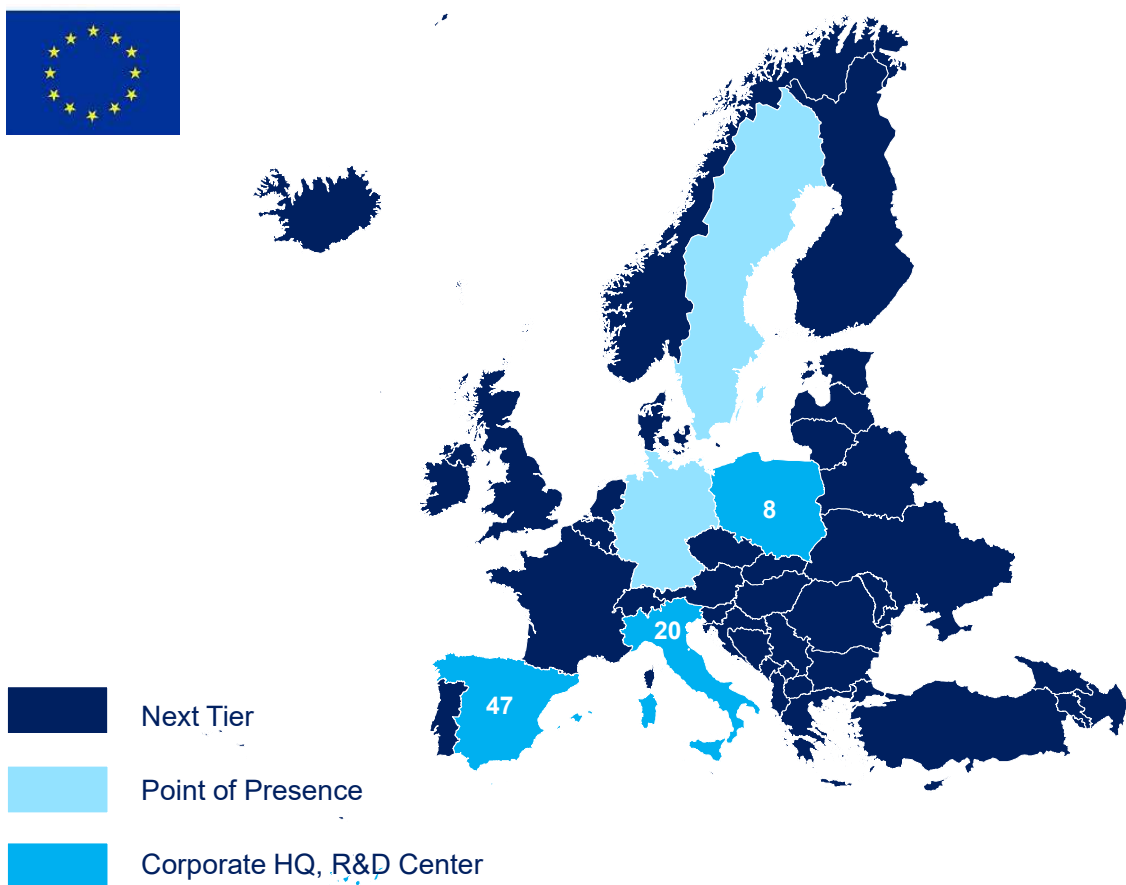


### Strategy for European Union Expansion

- Openchip is a European Project truly multinational and multicultural: Europe is in our DNA.

- We are determined to promote the collaboration within EU countries: Hiring a talented team, distributing R&D facilities and having a point of presence next to our priority customers.

- Company HQ is located in Barcelona, Spain, a global hub for business.

### OpenChip Presence

- OpenChip sites in Spain, Italy and Poland. 75 persons with fast growth.

- Plan a point of presence to articulate joint innovation with enabling customers across Europe

- Building a European leading company can only be possible by having a European mindset from European employees and European customers.

Next Tier

Point of Presence

Corporate HQ, R&D Center

# Openchip Strategy to Develop a Global Market

**Strategy for Global Expansion**

- Openchip will cultivate its alliances with Japan and US.

- Both countries are attractive as a market itself and count with very large Industrial partners that may use Openchip´s silicon portfolio in a wide variety of solutions for HPC, Cloud, Edge, Industrial IoT, etc.

- India, Brazil should be considered too.

**Next Steps**

- Plan a point of presence in Japan and US: Scouting mission in 2024.

- Asses India, Brazil and others.
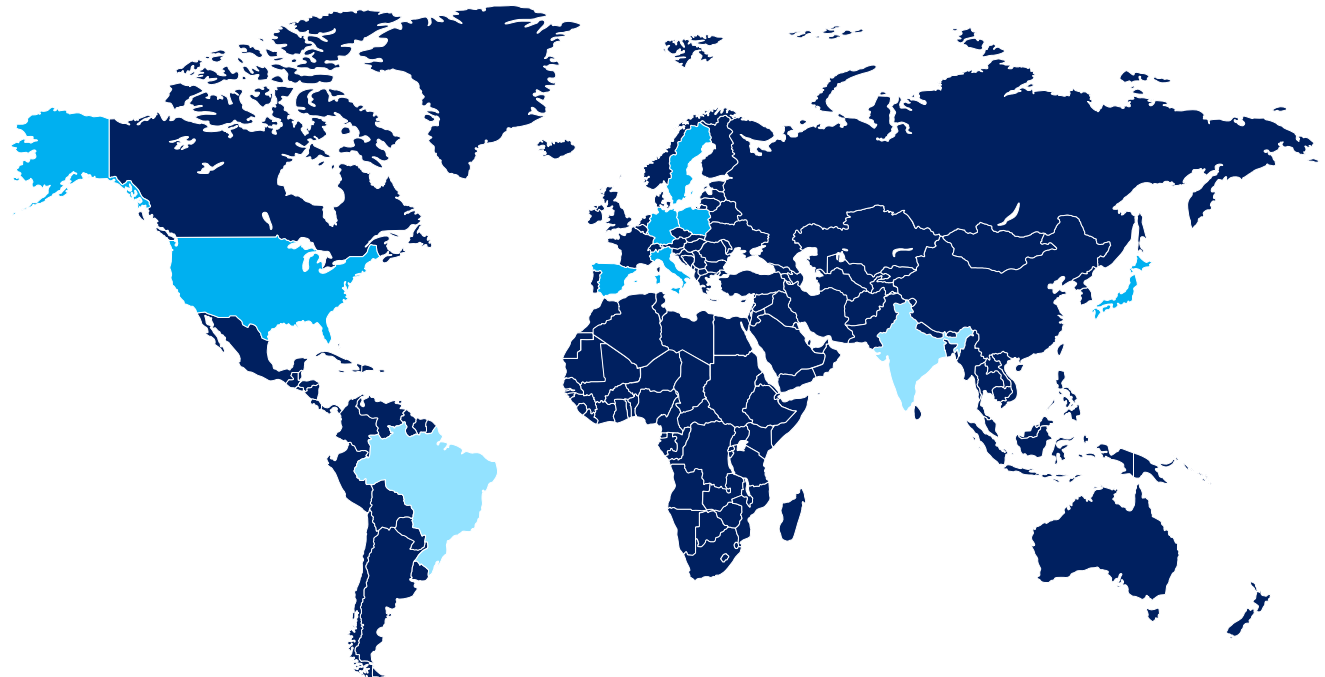
# Fabless Design House – Software & Hardware



Sales based on company headquarters location, % share

Legend: US, Taiwan, Europe, China, Rest of world

Categories (top to bottom): Equipment, Design software, Materials (excluding wafer), Materials (wafer), IP/EDA[1], Fabless, Integrated device manufacturers, Pure-play foundries, Semiconductor assembly, testing, and services

Capabilities up and down the value chain

[1]Intellectual property/electronic design automation.
Source: Gartner

# User & System Centric Mindset

User and Deployment Model Requirements

Workload Requirements and Service Level Objectives

SW and HW Codesign (power mgmt., orch., observability)

**Silicon Design**
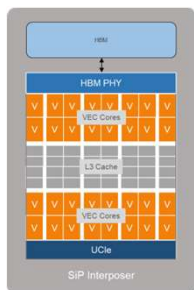
**PCB**

**Chassis & Advanced Cooling**

**Rack and Fabric**

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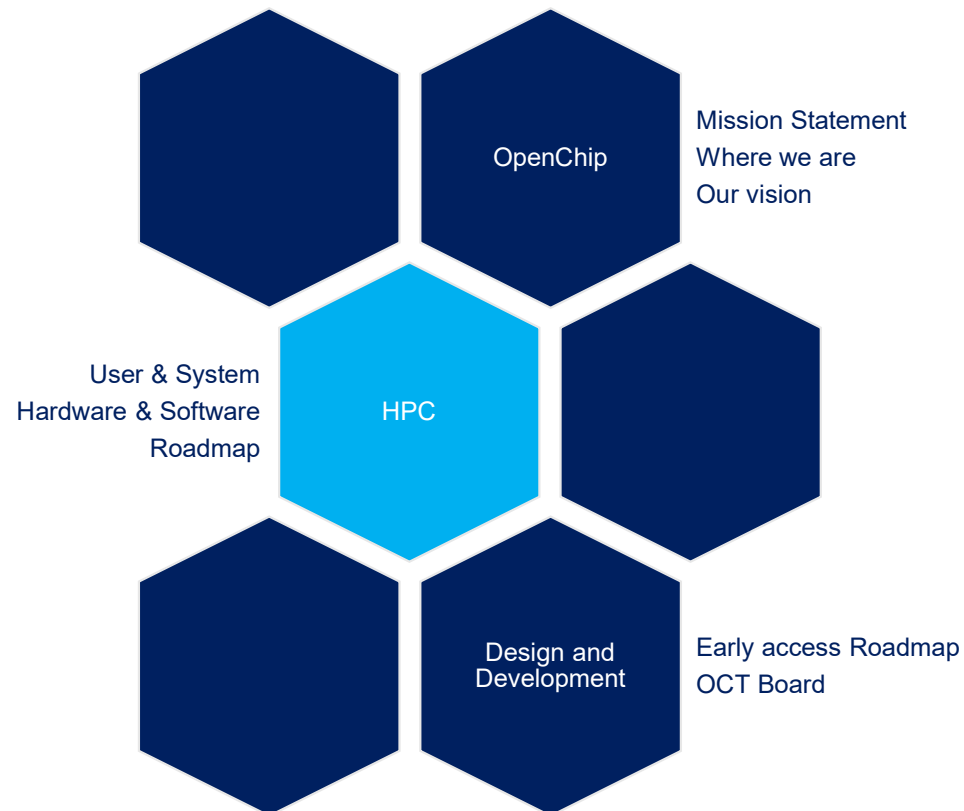
# OpenChip & HPC

Openchip´s first products launch

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AI-Focused HPC Server Revenue Forecast
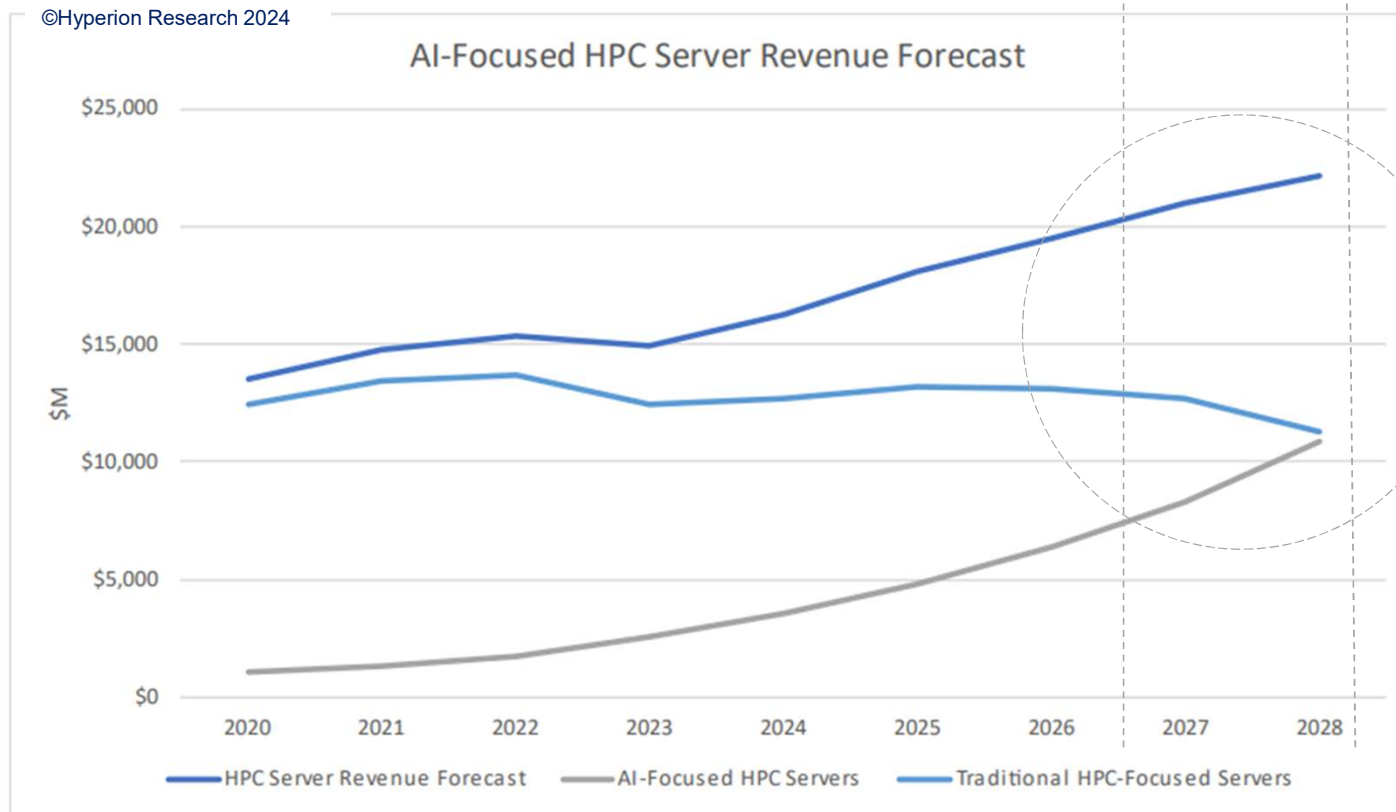
We are creating products today for a market that will change, HPC clusters will be a mix of heterogeneus computing resources.

Legend:
- HPC Server Revenue Forecast
- AI-Focused HPC Servers
- Traditional HPC-Focused Servers

NEC Aurora — Openchip

**From Ideas to Deployments: Creating the EU Chip for HPC & Vector Computing**

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- Chip companies use to *push* to the market their product offering, counting on a very reduced and **selected group of customers that influence** in the specs and collaborate in the testing & evaluation.
- **Openchip´s Advisory Board** (OAB) will be formed by a reduced number of selected customers with the willingness to collaborate to innovate the **EU Chip for HPC**; and eventually adopt it.
- OAB members will obtain a value by **accessing technology resources** both on premises and remotely that will allow them to validate and experience the potential benefits of **RISC-V Vector computing**.

| Market Research | Product Definition | Product Develop | Design Win | Demand Generation | Co-Selling | RFx | Delivery | Support |

Testing Samples — General Availability

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*It will be a **joint innovation** between **EU stakeholders**.*

*Only by our joint efforts we will be able to do a flagship **EU HPC Chip**.*

# Smooth transition to the new generation

**Aurora VE3**
- 4.9 FP64 TFLOPS (Vec)
- 370 W
- PCI form factor
- Near Mem 6 x HBM 2e

**VA_1000**
32-64 FP64 TFLOPS (Vec)
xx AI PFLOPS
500 - 1000 W
OAM/PCI form factor
Near Mem HBM

**VB_1000**
32-132 FP64 TFLOPS (Vec)
xx AI PFLOPS
400 - 1400 W
OAM/PCI form factor
Near Mem HBM

| 2024 | 2025 | 2026 | 2027 | 2028 | 2029 |

**NEC SX architecture**

VE controlling SW

Linux

X86 node

File system

SX Vector processor

core x 16

Memory

Vector Engine

**OC HPC architecture**

Linux

X86 node (optional)

File system

RISC-V Vector processor

core x 32

Memory

Memory

Linux

**SW continuity**

*Vector architecture achieves better memory BW utilization than GPU architecture*

* Subject to change

# Vector Chiplet



**Processing Unit (V)**
- CORE
- VPU
- L2

**SiP Interposer**
- HBM
- HBM PHY
- VEC Cores (V)
- L3 Cache
- VEC Cores (V)
- UCIe

OpenChip Gen1 VEC

OpenChip Gen2 VEC
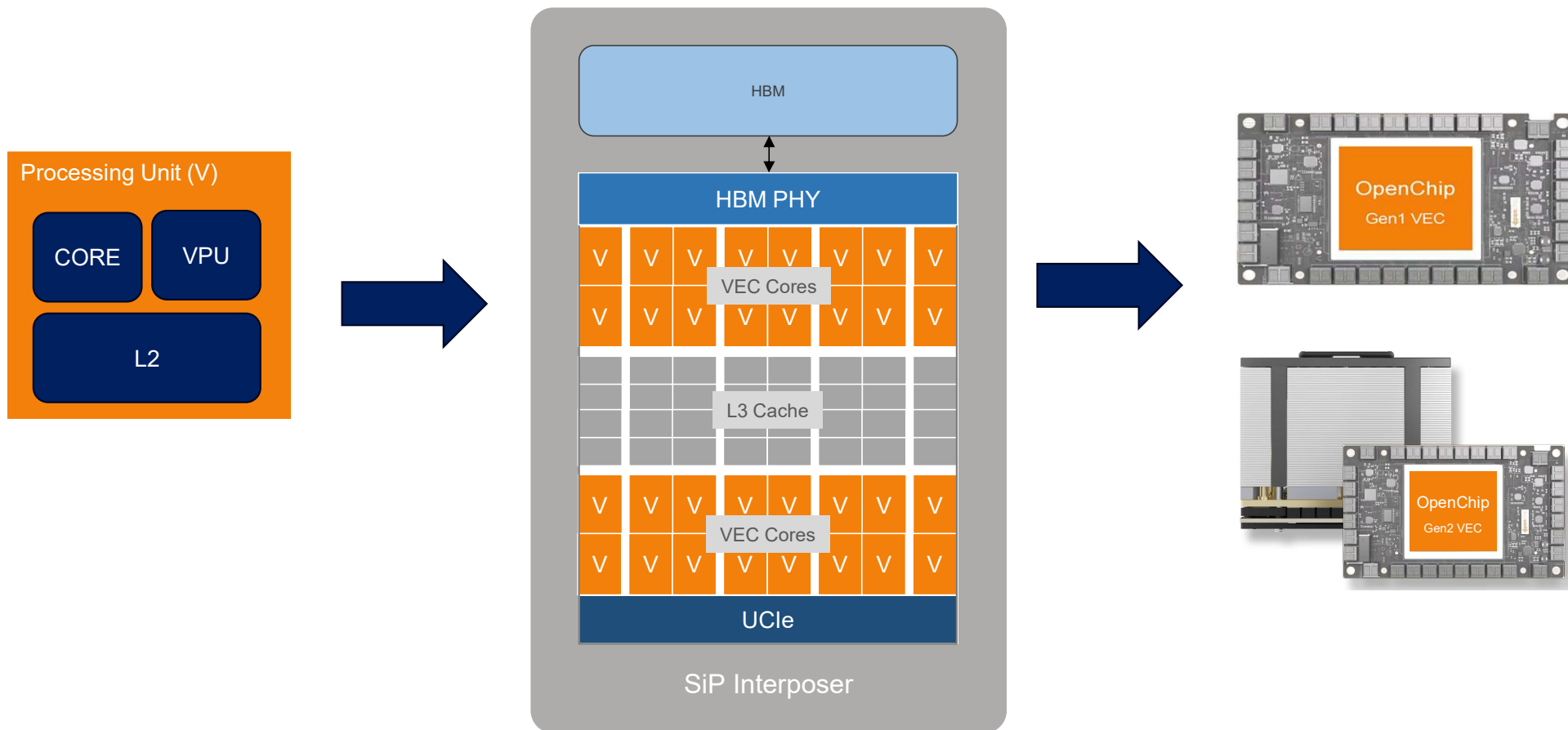
OpenChip HPC Software

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- Strictly Confidential -
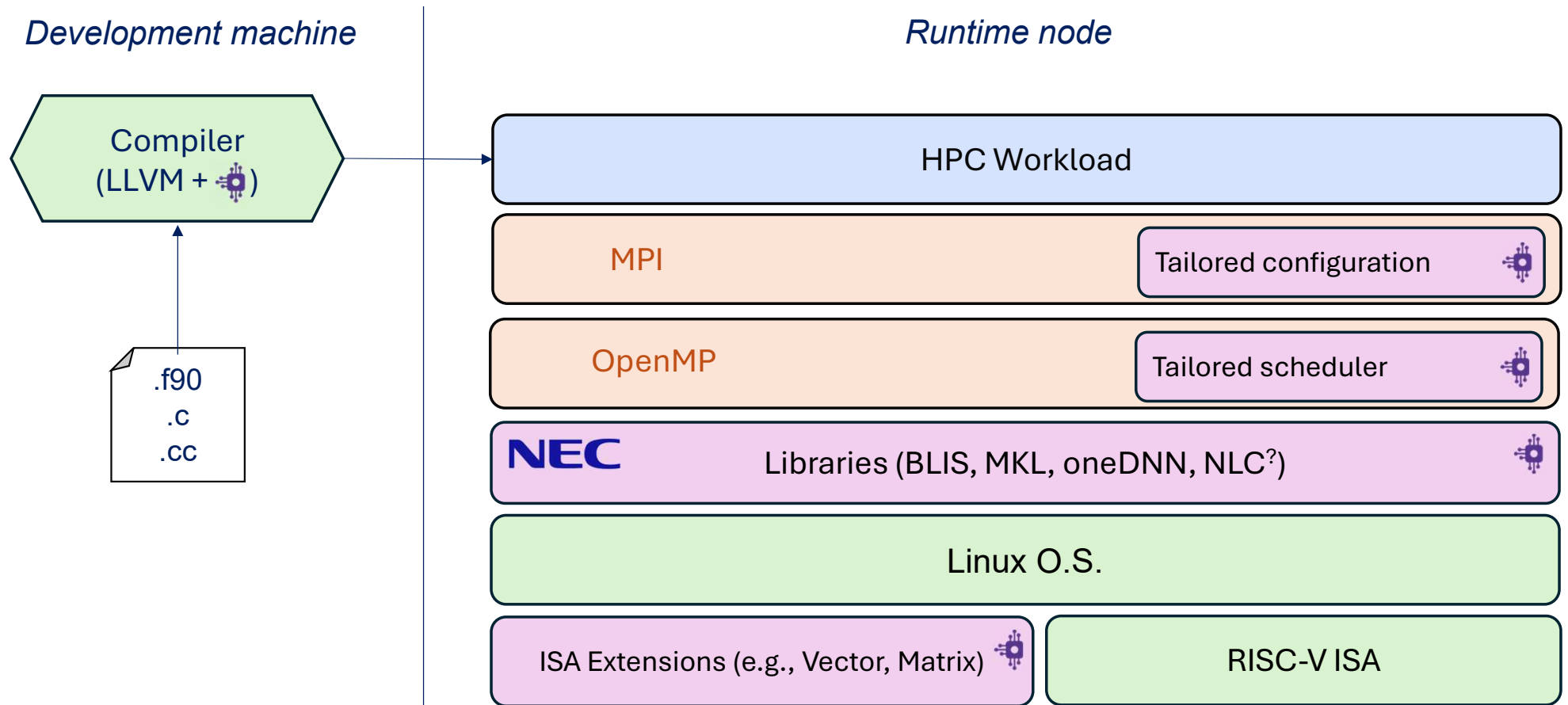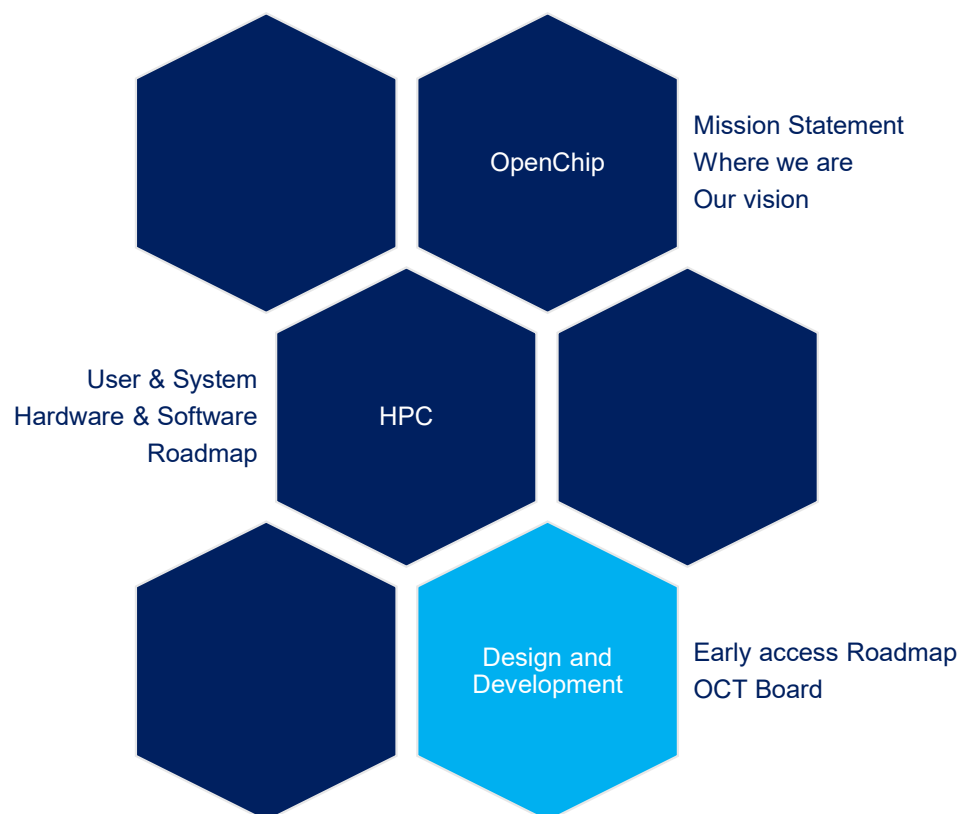
# Openchip´s Advisory Board for HPC
## Beyond a MOU

**Joint Innovation**

**Memorandum of Understanding**

Depth of Collaboration

• Identify common interests
• Seize the potential opportunity
• Draft a business-case: gives and gets
• Have a regular strategic discussion
• Gather requirements of future products
• Resources dedicated on a best-efforts

• Define a common Innovation Plan.
• Identify key specifications & functionalities.
• Intellectual Property prioritization.
• Potential agreements for IP onboarding and royalties fee income back.
• Resources committed to specific innovation activities, including R&D.
• Define a Governance Model for a periodical review.
• Laboratory facilities, equipment, etc.
• Case study & publications, dissemination.
• Marketing and Communication, PR
• Co-investment of resources: Testing equipment, engineering, etc.

*Non-Binding Collaboration*                    *Advisory Board HPC: Co-Innovation*

### Governance

• **Openchip**: Host & Sponsor.
• **NEC**: Technology Partner.
• **Steering Committee**: 5 to 7 members of HPC.
• 1 meeting per quarter.
• Format:
  • Offsite f2f workshops.
  • Location: Countries within EU.
  • Disclose plans.
  • Receive feedback.
  • Identify and prioritize key features.
• Resources:
  • Remote Hosted Lab.
  • Technical support.
  • On premise seed units.
• Additional benefits:
  • Early access to new products.
  • Potential new IP agreements: Co-Developments, etc.
• Terms & Conditions:
  • No cost, no entry fee, no maintenance.
  • Affiliate Agreement (incl. NDA, etc)
  • Cost of resources by Sponsor.
• Next Steps:
  • Please tell us about your interest!
  • 1st f2f session September.

# Openchip Advisory Board HPC Timeline & Expected Results



**First SD Silicon Platform**

Simulation of first design available remotely via Software Developer Cloud at the end of the year. Activate next phase of software testing and advanced porting activities.

**Advisory Board HPC**

Open call to participate to leading Euro HPC during NEC User Group

**Packaging, Testing**

System integration and testing.
Quality control
Software developments continue
Early access program

**2nd OpenChip GA**

Commercially available

| 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 |

**NEC & Openchip**

**Initial Plan**

First MOU & Strategic Collaboration framework

**Early Access SDK**

Remote access to a testing facility to assess technology
Remote technical support.
Identify key algorithms to test
Support a few porting activities

**First Tape-out**

After a deep testing to ensure the best quality, OC will do the first Tape-Out.

**1st OpenChip GA**

Commercially available

# Openchip & NEC, a truly Partnership

THANKS!

# BACKUP